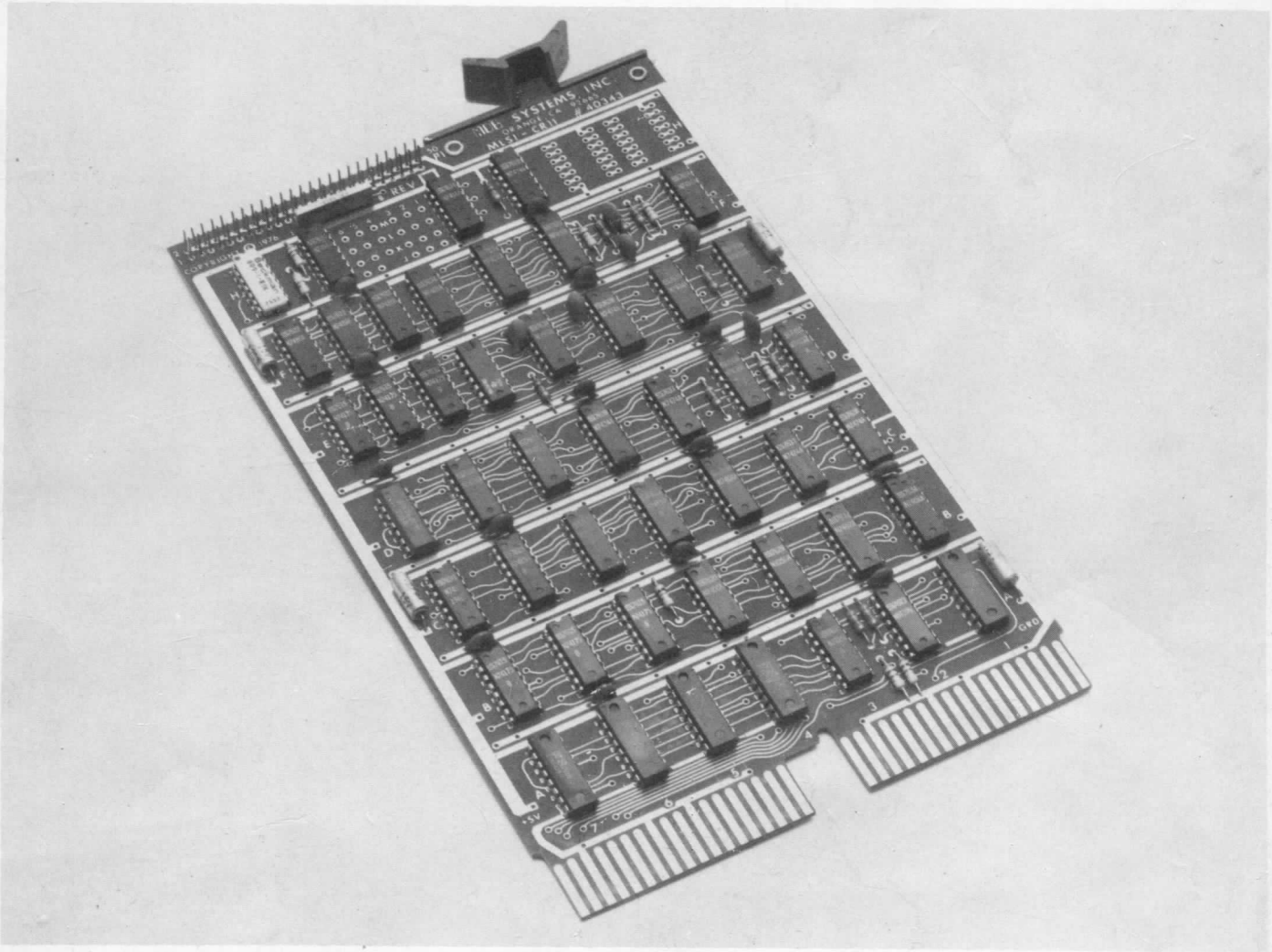
MDB

MLSI-CR11

CARD READER CONTROLLER

INSTRUCTION MANUAL

☐ DATA 100 ☐ DOCUMENTATION ☑ OTHER TRU-DATA



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MLSI-CR11 CARD READER CONTROLLER

INTRODUCTION

The MLSI-CR11 Card Reader Controller (called simply the Controller in this manual) controls the transfer of data from a card reader to the data bus of a DEC KD11-type processor. The Controller is easily adapted, using wire jumpers, to operate with a variety of different card readers. It is especially designed to interface with Documentation and DATA 100 card readers.

Under software control, card reader data may be selected to the bus in either the standard 12-bit Hollerith code, or in the 8-bit compressed Hollerith code.

The Controller is built on a single dual module to be installed in an MDB BPA-84 Backplane/Cardguide Assembly, and is completely compatible with existing DEC operating and diagnostic software written for use with the DEC PDP-11/03.

Figure 1 shows the position of the Controller in the system.

PHYSICAL DESCRIPTION

The Controller is built on a single DEC-type dual module that can be plugged into one of the 16 dual slots in an MDB BPA-84 Backplane/Cardguide Assembly. Power is applied through standard backplane connections made at the assigned post on the backplane terminal strip.

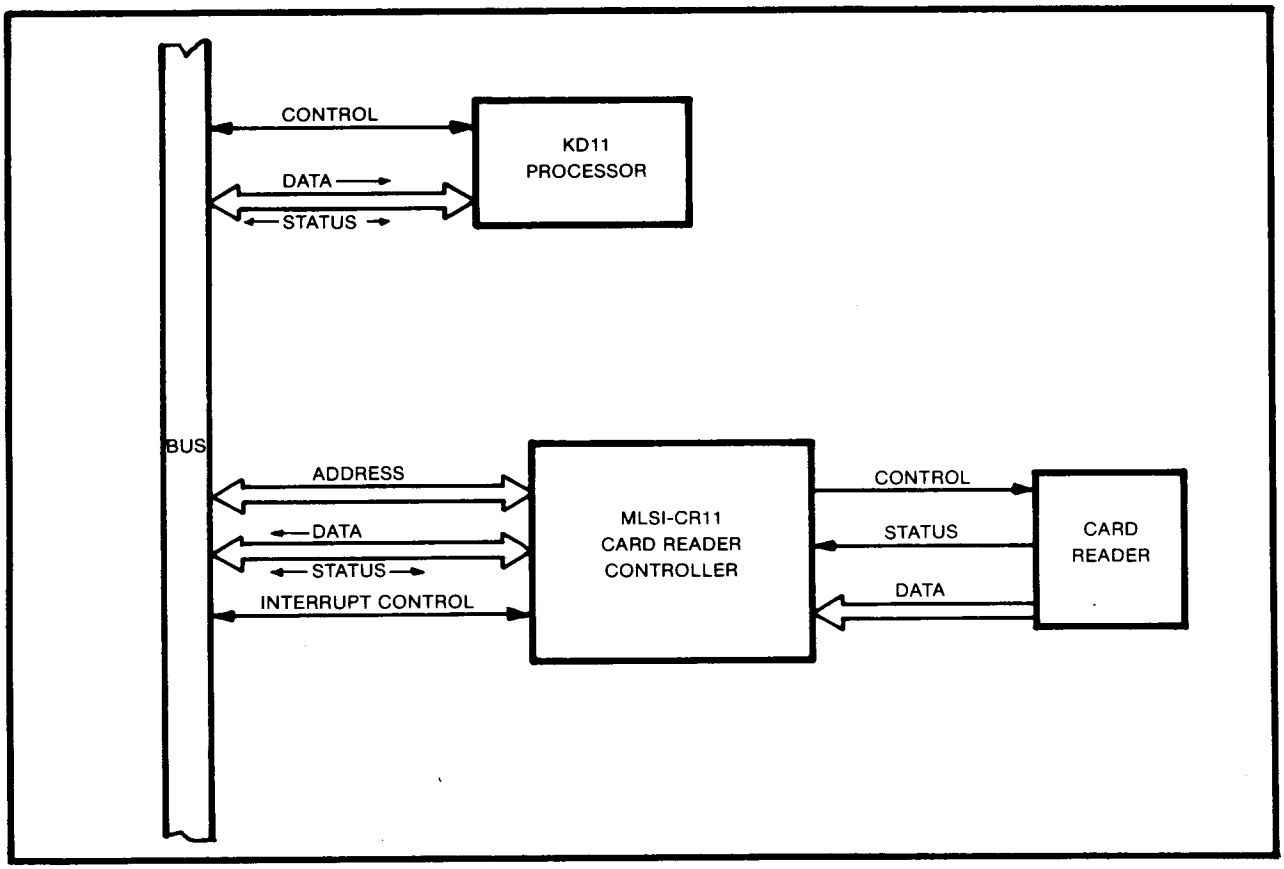


Figure 1. System Block Diagram

The Controller module has a single connector for connection to the card reader. An interface cable with mating connectors is supplied with the module.

INSTALLATION

The following paragraphs contain instructions and information for installing the Controller module, and for installing wire jumpers that configure the module for its specific application.

UNPACKING THE CONTROLLER

Carefully unpack the Controller printed circuit module, and inspect it for damage thoroughly before installation. If damage is apparent, retain the shipping material and promptly notify both MDB Systems and the carrier.

INSTALLING MODULE

Plug the module into any available dual module slot in the MDB BPA-84 Backplane/Cardguide Assembly at a selectable priority in the interrupt daisy chain. Figure 2 shows priority flow and the slot arrangement in the Backplane Assembly.

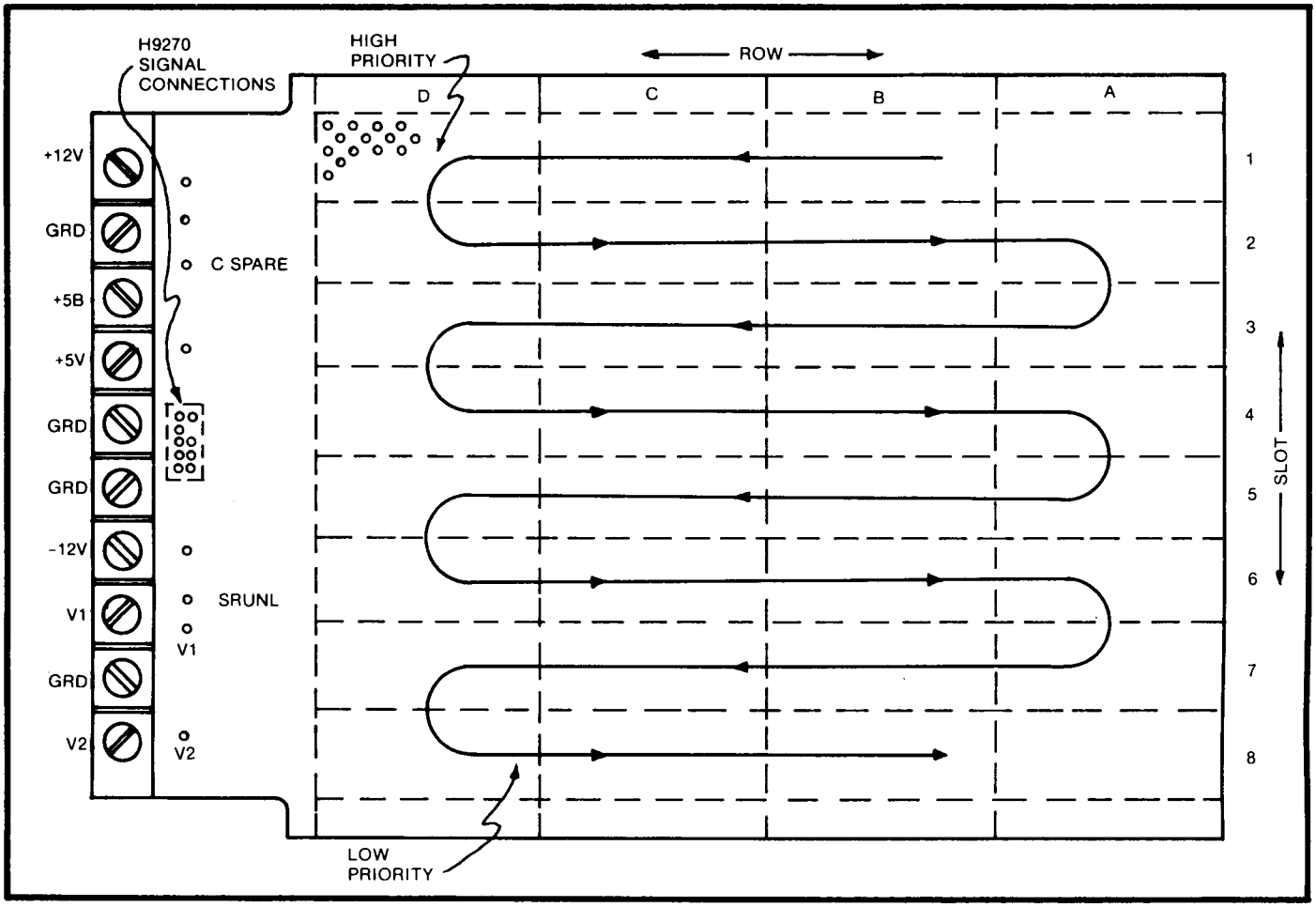


Figure 2. Typical Controller Mounting

CABLING

The cable from the card reader may be brought directly to connector P1 on the Controller module, and connected to the module so that the highlighted arrows are facing one another. The card reader end of the cable mates directly with the card reader connector. Table 1 lists pin connections for connector P1 on the Controller module.

Table 1. Card Reader Cable Connector (J1)

Pin	Signal	Pin	Signal
1	Row 12 DATA	26	INDEX MARK Return
2	Row 12 Return	27	READY
3	Row 11 DATA	28	READY Return
4	Row 11 Return	29	ERROR
5	Row 0 DATA	30	ERROR Return
6	Row 0 Return	31	HOPPER CHECK
7	Row 1 DATA	32	HOPPER CHECK Return
8	Row 1 Return	33	MOTION CHECK
9	Row 2 DATA	34	MOTION CHECK Return
10	Row 2 Return	35	PICK
11	Row 3 DATA	36	PICK Return
12	Row 3 Return	37	CARD IMAGE
13	Row 4 DATA	38	CARD IMAGE Return
14	Row 4 Return	39	Ground
15	Row 5 DATA	40	Ground
16	Row 5 Return	41	Ground
17	Row 6 DATA	42	Ground
18	Row 6 Return	43	Spare
19	Row 7 DATA	44	Ground
20	Row 7 Return	45	Spare
21	Row 8 DATA	46	Ground
22	Row 8 Return	47	Ground
23	Row 9 DATA	48	Ground
24	Row 9 Return	49	Ground
25	INDEX MARK	50	Ground

JUMPER CONNECTIONS

Certain jumper connections may be prepared on the module in order to configure the Controller to operate with the specific card reader.

The Controller is furnished with all card reader interface lines configured positive-true. The logic sense of the card reader data is determined by jumper J/5-6 as follows:

High-true = jumper J/5-6 omitted.
Low-true = jumper J/5-6 installed.

Referring to sheet 3 of the logic diagram in this manual, connect jumpers as required to select card reader status signals to be set in the Status Register, and the true level of each signal. Control and status signals to be jumpered are as follows:

Signal	Jumper High-true	Jumper Low-true
PICK	J/2-1	J/2-3
INDEX MARK	M/5-6	M/5-4
MOTION CHECK	L/2-1	L/2-3
ERROR	K/5-6	K/5-4
HOPPER CHECK	M/2-1	M/2-3
READY	L/5-6	L/5-4
CARD IMAGE	K/2-1	K/2-3

PROGRAMMING INFORMATION

REGISTERS

Software control is performed by two registers in the MSLI-CR11, which are addressed by four addresses.

The Data Buffer Register, a read-only register, stores data from one card column. It may be addressed as a 12-bit register (standard Hollerith code), or as an 8-bit register (compressed Hollerith code).

The Status Register, a read/write register, holds card reader status for transfer to the bus; and holds the Interrupt-Enable bit (bit 06), and Eject and Read bits (bits 01 and 00), output by the program to the bus.

Table 2 lists the registers and their addresses.

Table 2. Device Register Addresses

Register	Mnemonic	Address
Status (read)	CRSI	777160
Status (write)	CRSO	777160
Data Buffer (12 bits)	CRB1	777162
Data Buffer (8 bits)	CRB2	777164

Status Register

Different card readers may supply different status signals, or signals of different logic sense (high-true or low-true). Jumpers on the module may be changed to adapt the module for use with different card readers (refer to *Jumpers*). An unused status bit must be read as a "0".

Note that (figure 3) because data is never written in the high-order byte, status is to be written using only word addressing, or low-order byte addressing. Table 3 lists and describes each bit in the Status Register.

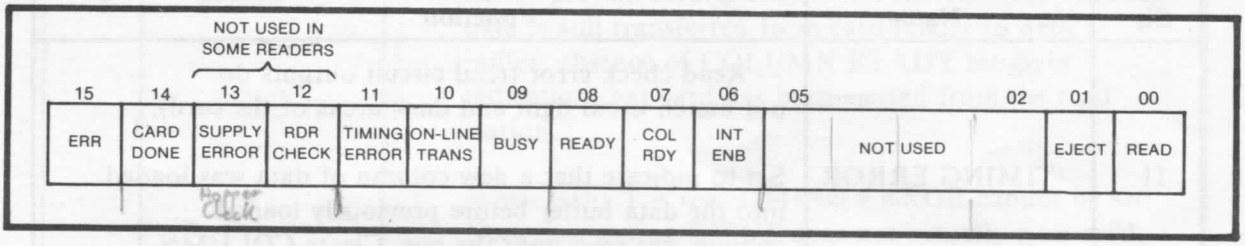


Figure 3. Status Register Bit Assignments

Table 3. Status Register Bits

Bit	Name	Function
15	ERROR	Set to indicate an error condition, when either of the following conditions occurs: — The card reader goes off-line, normally when a card check (MCK) or hopper check (HCK) error is sensed. — A timing error is sensed when the reader finishes reading a card (Card Done). Subsequent Read commands are ignored until ERROR has been cleared. ERROR is used by interrupt logic to direct the program to an error-handling routine. After ERROR is cleared, bits 15, 14, 11, and 10 are automatically cleared when status register is loaded.
14	CARD DONE	Set to indicate that the next card may be taken from the input hopper. Bit is used at interrupt logic. Read-only bit, cleared by INIT or by loading the Status Register.
13	HOPPER CHECK	Set to indicate that either input hopper is empty, or output stacker is full. Operation cannot proceed until condition is corrected. If either signal is not supplied by card reader, be sure respective jumper is correctly installed (refer to *Jumpers*).
12	CARD READER CHECK	Set to indicate that an abnormal condition has been detected as card was read, as follows: — Feed check error (card was not delivered to read station).

Table 3. Status Register Bits (cont'd)

Bit	Name	Function
		— Read check error (read circuit outputs do not match usual light and dark areas of the card).
11	TIMING ERROR	Set to indicate that a new column of data was loaded into the data buffer before previously loaded column was read onto the bus. Clears COLUMN READY bit, and causes ERROR bit to be set. COLUMN READY bit cannot be set until bit 11 is cleared. Bit 11 cannot be set if EJECT bit is set.
10	READER TRANSITION TO ON-LINE	Set to indicate that the card reader has gone on-line. Card reader goes off-line if an error condition is detected or STOP switch is pressed. Bit 10 appears at interrupt logic to indicate that card reader is available. Read-only bit, cleared by INIT or by loading status Register.
09	BUSY	Set to indicate that a card is being read.
08	READER READY	Set to indicate that card reader is *off-line.* Cleared, indicates that card reader is on-line and able to accept commands. Read-only bit.
07	COLUMN READY	Set to indicate that one column of data has been loaded into data buffer and is ready for transfer to the bus. Bit 07 cannot be set if a card is ejected or a timing error occurs. Cleared when data buffer is addressed. Appears at interrupt logic so that program can transfer the data. Read-only bit, cleared by INIT or by addressing data buffer.
06	INTERRUPT ENABLE	Set to allow interrupt to occur if any of the following status bits is set: 15, 14, 10, or 07. Read/Write bit, cleared by INIT.
05 - 12	not used	

Table 3. Status Register Bits (cont'd)

Bit	Name	Function
01	EJECT	Set to prevent setting COLUMN READY bit. Although data is still transferred from card reader to data buffer, absence of COLUMN READY bit gives indication that card has been ejected from the read station. When EJECT is set, TIMING ERROR cannot be set. Note that setting EJECT does not actually eject card, unless READ bit is also set. Read/Write bit, cleared by INIT.
00	READ	Set to cause card reader to deliver a card to read station. Cleared by INIT or by program loading "0". Can be read but is read as "0" regardless of actual state.

Data Buffer Register

The 12-bit Data Buffer Register receives the 12 bits read from each column of the card. As the data settles on the lines, the card reader asserts COLUMN INDEX to load the data into the buffer.

The contents of the data buffer are read onto the bus, addressed by the decoded address code CRB1 or CRB2. If CRB1 is decoded, the 12 bits are gated to the bus without conversion, with the least-significant bit appearing as bit 00.

If CRB2 is decoded, the five most-significant bits are gated to bus lines 07 through 03. The seven least-significant bits, however, are applied to conversion logic providing a 3-bit output gated to lines 02, 01, and 00.

Figure 4 shows bit assignments in the Data Buffer Register.

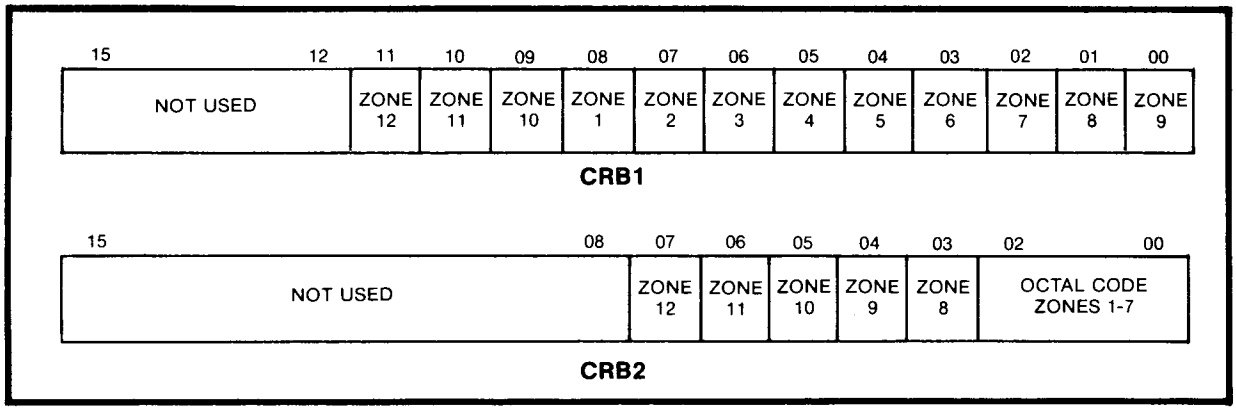


Figure 4. Data Buffer Register Bit Assignments

INTERRUPT VECTOR ADDRESS

The interrupt vector address is hardwired on the Controller module and is 230.

THEORY OF OPERATION

GENERAL

The following pages describe the function of each line at the Controller/bus interface, and at the Controller/card reader interface, and describes the basic operating cycle for transferring data from the card reader to the bus.

For more detailed information, refer to the logic diagrams included in this manual, and to appropriate manuals for the KD-11 processor and the card reader.

CONTROLLER/BUS INTERFACE

Table 4 lists and defines signals at the Controller/bus interface.

Table 4. Bus/Controller Interface Signals

Signal	Description
BIRQL	Interrupt request generated by Controller. Asserted to inform processor of data to be input, or output data to be accepted. Program status word bit 6 must be false in order for the interrupt request to be acknowledged by BIAKOL.
BRPLYL	Reply, generated by Controller in response to either BDINL or BDOUTL, indicating that either input data is available on the bus, or output data on the bus has been accepted.
BIAKIL, BIAKOL	Interrupt acknowledge signal from processor to system modules, in response to interrupt request BIRQL. If module is not generating the interrupt request, BIAKIL passes through the module to the BIAKOL line.
BSYNCL	Synchronize. Received from processor when it places an address on data lines BDAL0L-BDAL15L.
BDINL	Data input signal, received when BSYNCL is asserted to indicate that the processor is performing an input transfer. When BSYNCL is not asserted, BDINL implies that an interrupt operation is in progress.
BDOUTL	Data output signal implying that valid data is on data bus, and that processor is performing an output transfer. Device responding to BDOUTL must assert BRPLYL to complete the data transfer.
BBS7L	Bank 7 Select. Asserted by processor to indicate that an address in the upper 4K bank (25K-32K) is on the bus. If BSYNCL is asserted, BBS7L remains active until bus cycle addressing is completed.
BINITL	Initialize. Generated by processor during power-up to clear all devices on the I/O bus.
BDAL0L-BDAL15L	Data/Address bus, bidirectional, over which all address and data information is transferred.

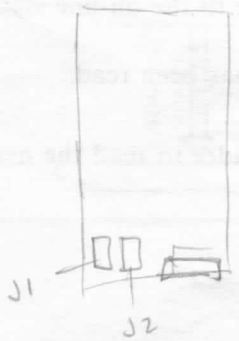
CONTROLLER/CARD READER INTERFACE

Table 5 lists and defines signals at the Controller/Card Reader interface. Refer to table 1 for connector pin assignments, and to table 3 for status bit functions set by selected status signals.

Logic levels (high-true or low-true) depend on the specific card reader type and may be selected using jumpers on the Controller module.

Table 5. Controller/Card Reader Interface Signals

Signal	Source	Description
ROW 1 DATA through ROW 12 DATA	Card Reader	Hollerith-coded data read from one column of the card, and strobed into the Data Buffer Register by INDEX MARK.
INDEX MARK	Card Reader	Pulse occurring when column data has settled on the data lines. Strobes data into the Data Buffer Register.
PICK	Controller	Requests card reader to pick and read a card. Asserted by bit 00 with CRSO command. Cleared by INITL or INDEX MARK pulse.
MOTION CHECK	Card Reader	Indicates that card was not delivered to read station in response to PICK command. May set CARD READER CHECK bit in Status Register.
ERROR	Card Reader	Indicates that a reading error has occurred in a column of data. May set ERROR bit in Status Register.
HOPPER CHECK	Card Reader	Indicates that the feed hopper is empty. Operation cannot resume until cards are placed in hopper. Sets HOPPER CHECK bit in Status Register.
READER READY	Card Reader	Indicates that card reader is on-line and able to accept feed commands. Sets READER READY bit in Status Register.
CARD IMAGE	Card Reader	Indicates that data column portion of card is at the read station. Sets BUSY bit in Status Register.



OPERATING CYCLE

Figure 5 shows the general organization of the Controller.

The device address on the bus is loaded into the address register when the processor asserts BSYNCL. When either a BDOUTL or BDINL command is asserted at the bus, the address decoder is enabled, and address bits 01 and 02, and the state of DATOUT, are decoded to cause one of four register-select signals to go low, as follows:

a. CRSI, to transfer the contents of the Status Register to the bus.

b. CRSO, to load bits 00, 01, and 06 from the bus into the Status Register.

c. CRB1I, to transfer a 12-bit Hollerith-coded character to the bus.

d. CRB2I, to transfer an 8-bit compressed-Hollerith-coded character to the bus.

The Controller acknowledges receipt of either BDOUTL or BDINL, after a short delay, by asserting BRPLY. BRPLY is also asserted to notify the processor that the interrupt vector address has been placed on the bus.

When data is to be placed on the bus, the Status Register is first addressed and loaded (bit 00) to provide a READ (PICK) command to the card reader. The card reader then either reads and transfers the next data column or, if the last card has been completed, picks a new card, and reads and transfers the first data column. The Controller then sets COLUMN READY in the Status Register and sets an interrupt (BIRQL).

The processor responds to the request by asserting BDINL and BIAKIL, the Controller puts its vector address on the bus, and the processor accepts the contents of the Data Buffer Register. The READ bit is again set in the Status Register to initiate the next cycle.

If CRB1 is specified, the 12-bit column data appears on the bus lines unchanged. However, if CRB2 is specified, the column data is compressed onto eight lines. Compression is performed by converting the seven least-significant bits of column data into a 3-bit octal code.

A CRSO command may load any of three bits into the Status Register, as follows:

a. **Interrupt Enable (BDAL06L)** — INT ENB enables the Controller to set an interrupt whenever one of the following events occurs:

1. An ERROR occurs, or

2. the card reader goes from an off-line state to the on-line state, or

3. a card data column, or a complete card, has been read.

b. **Read (BDAL00L)** — READ causes the card reader to read the next data column, or the next card.

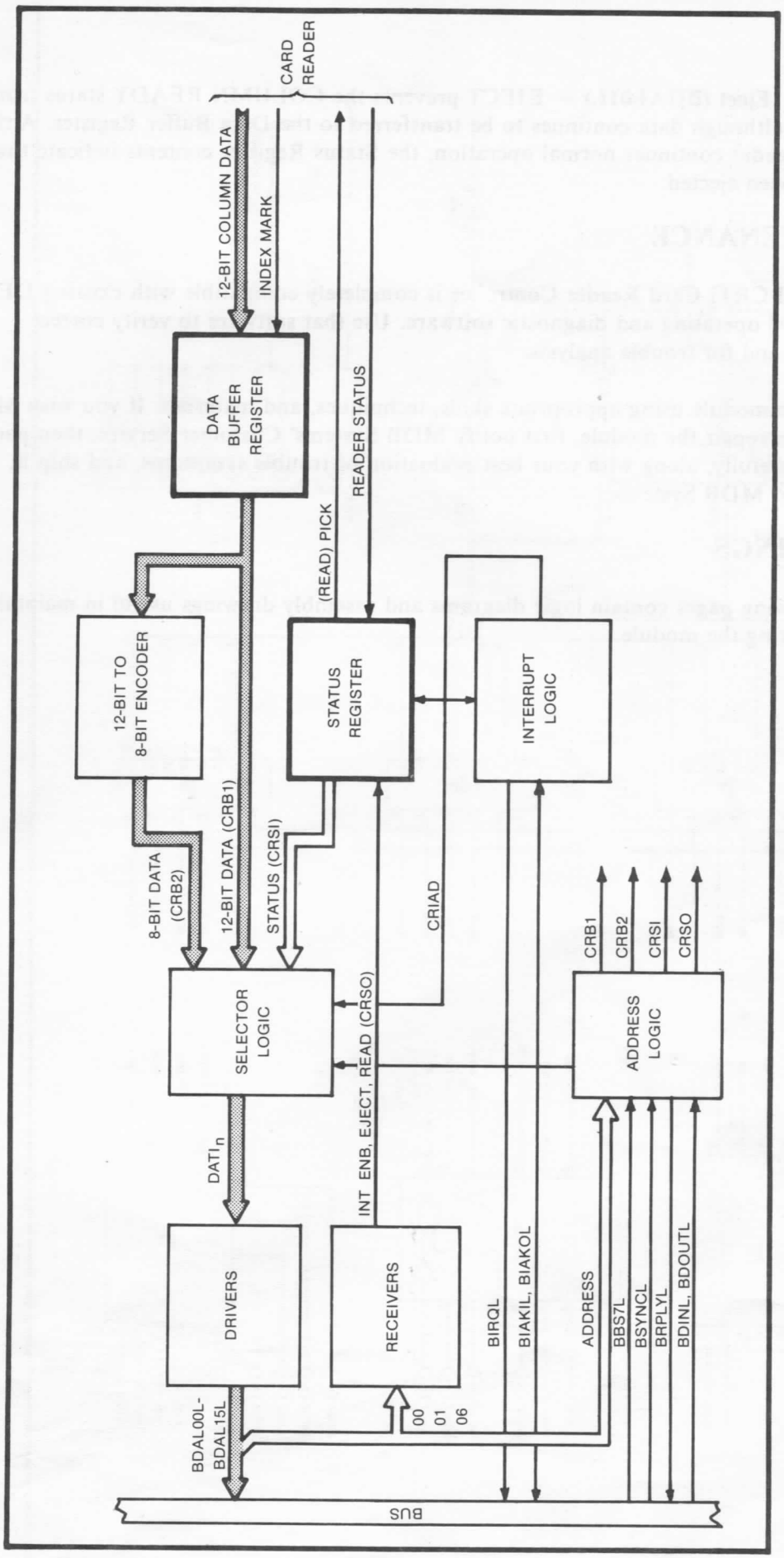


Figure 5. MLSI-CR11 Card Reader Controller, Simplified Block Diagram

c. **Eject (BDAL01L)** — EJECT prevents the COLUMN READY status from being set, although data continues to be transferred to the Data Buffer Register. Although the card reader continues normal operation, the Status Register contents indicate that the card has been ejected.

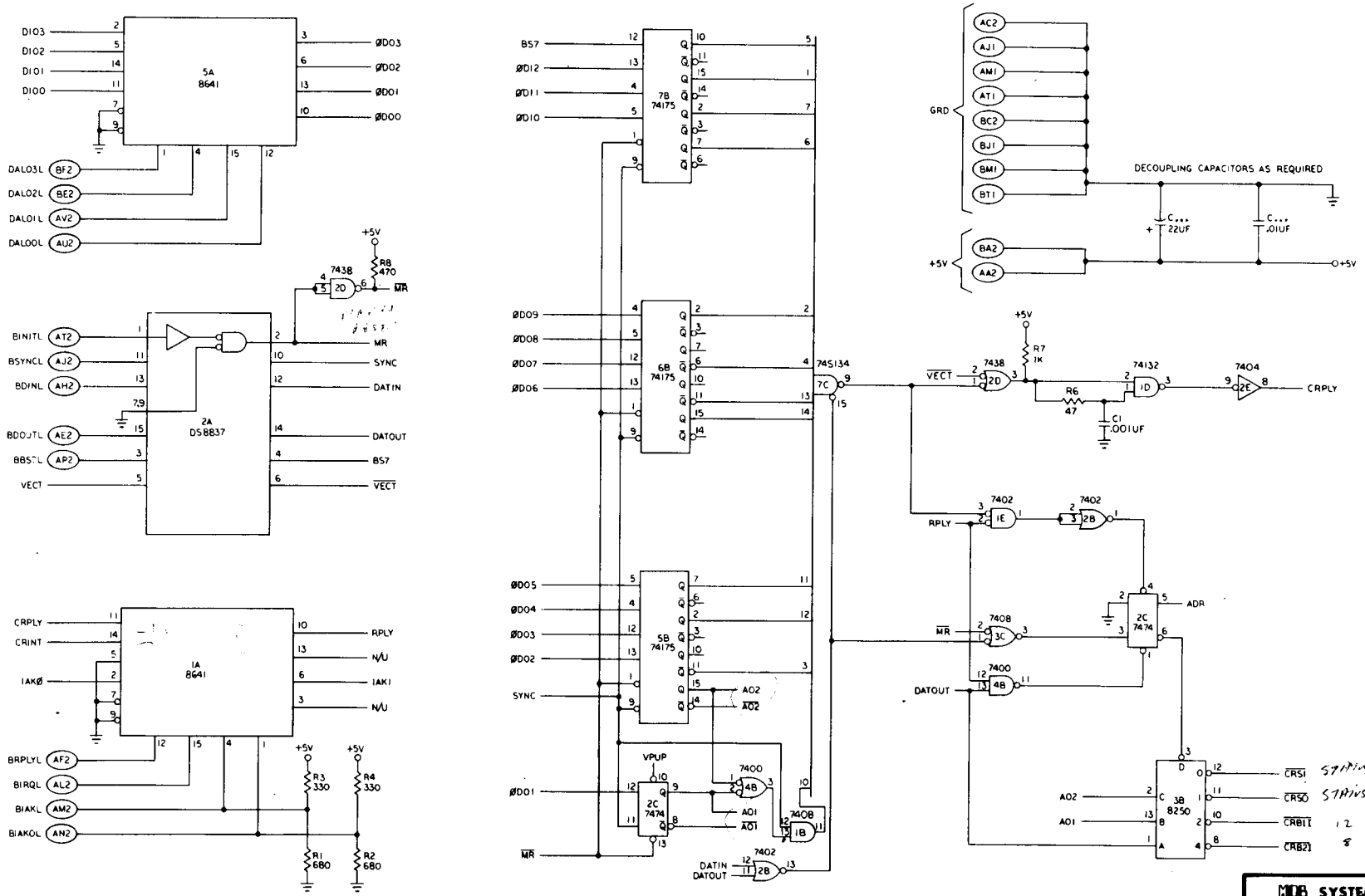
MAINTENANCE

The MLSI-CR11 Card Reader Controller is completely compatible with existing DEC PDP-11/03 operating and diagnostic software. Use that software to verify correct operation and for trouble analysis.

Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, first notify MDB Systems' Customer Service, then pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems.

DRAWINGS

The following pages contain logic diagrams and assembly drawings useful in maintaining and repairing the module.



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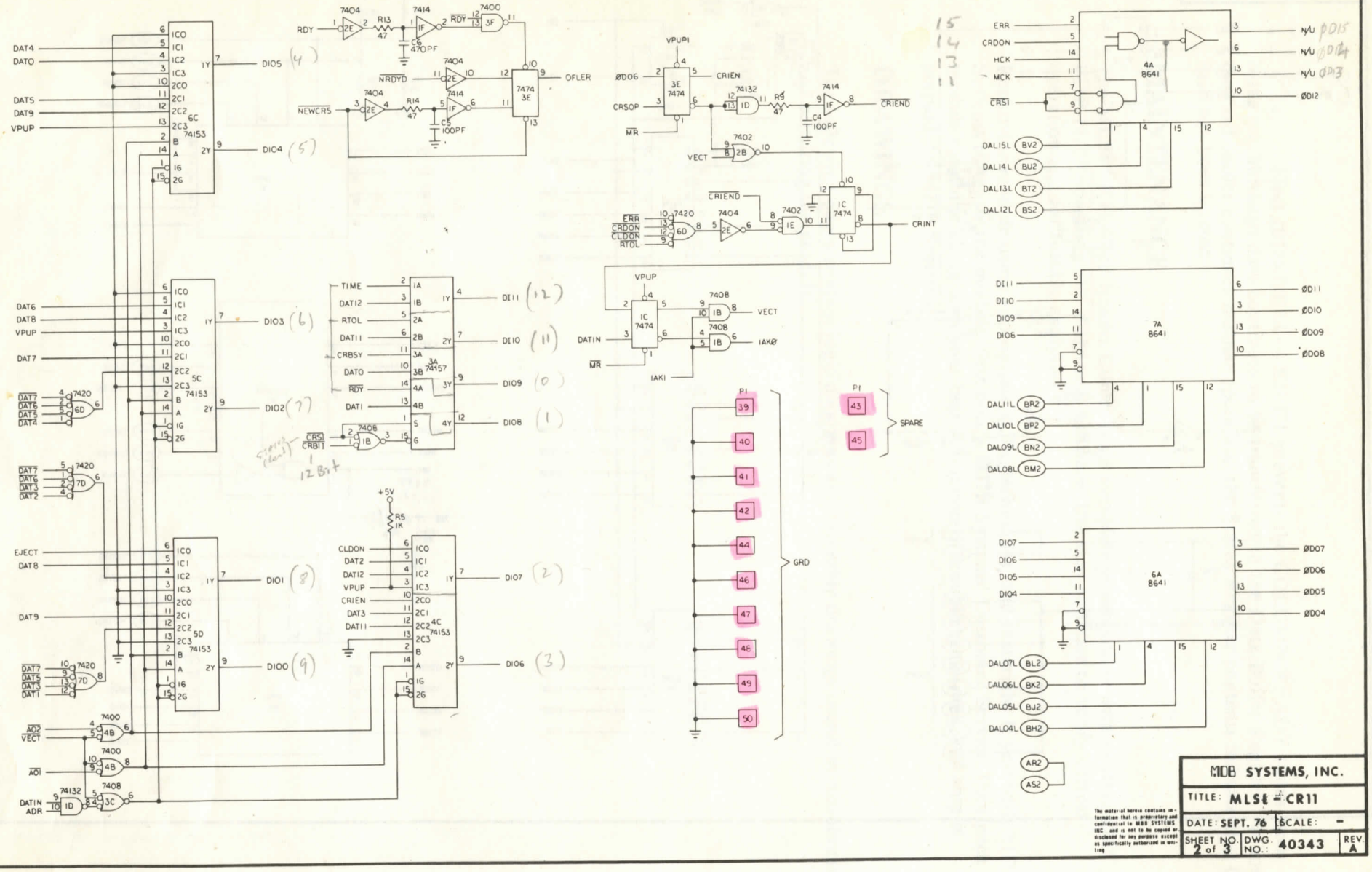
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DAT5
DAT9
VPUP
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DIO4 (5)
RDY
NEWCRS
OFLER
NRDYD
DAT6
DAT8
DAT7
DIO3 (6)
DIO2 (7)
TIME
DAT12
RTOL
DAT11
CRBSY
DATO
DATI
DII (12)
DIO (11)
DIO9 (0)
DIO8 (1)
CRS
CRBI
12 Bit
EJECT
DAT8
DAT9
DIO1 (8)
DIO0 (9)
CLDON
DAT2
DAT12
VPUP
CRIEN
DAT3
DAT11
DIO7 (2)
DIO6 (3)
+5V
R5
1K
AO2
VECT
AO1
DATIN
ADR
ØD06
CRSOP
MR
CRIEN
CRIEND
VECT
ERR
CRDON
CLDON
RTOL
CRINT
VPUP
DATIN
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DAL12L BS2
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DIO
DIO9
DIO6
ØD11
ØD10
ØD09
ØD08
DAL11L BR2
DAL10L BP2
DAL09L BN2
DAL08L BM2
DIO7
DIO6
DIO5
DIO4
ØD07
ØD06
ØD05
ØD04
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DAL06L BK2
DAL05L BJ2
DAL04L BH2
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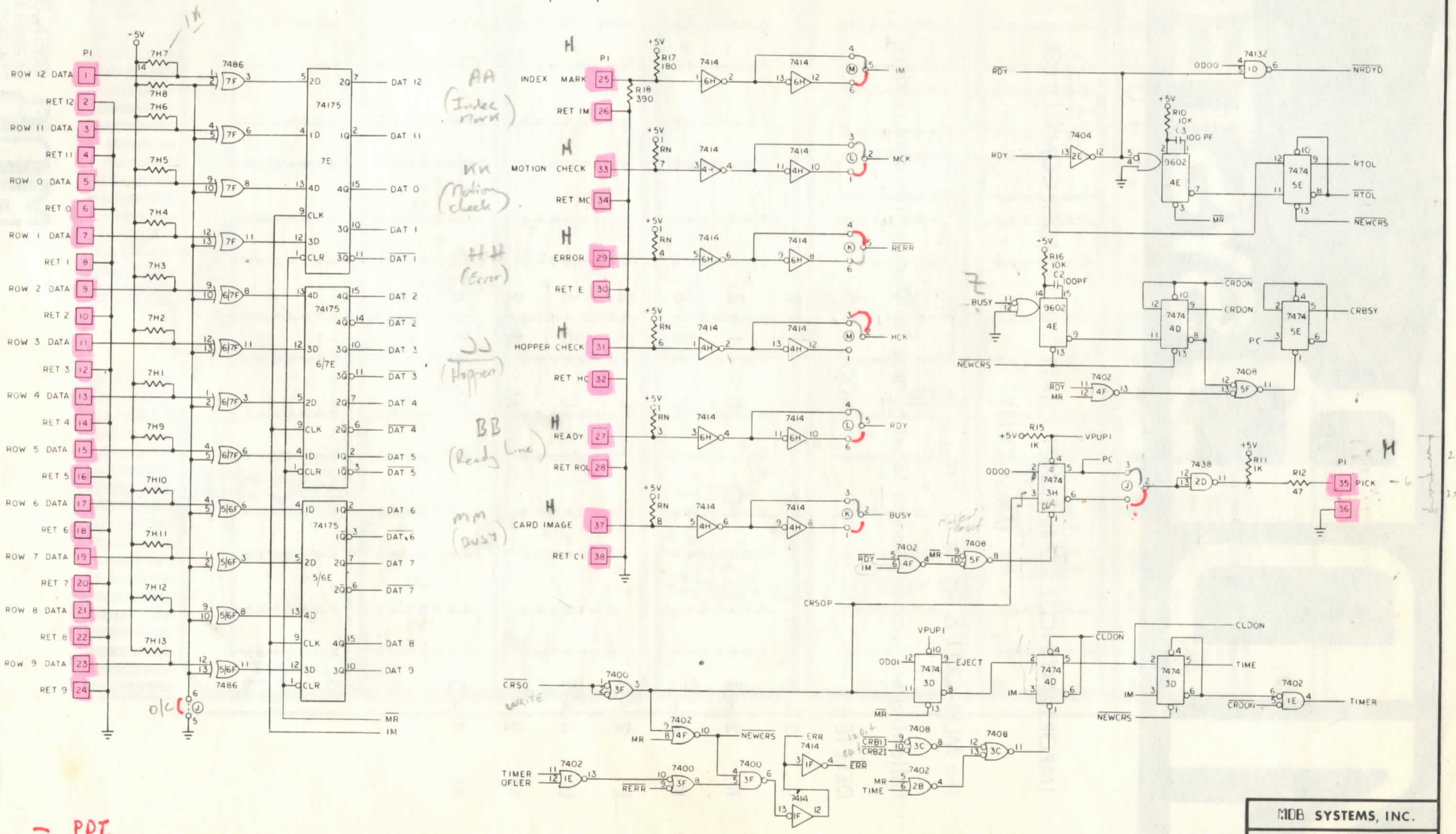

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IMPORTANT NOTE TO USERS OF LSI-11 CARD READER CONTROLLER :

(MLSI-CR11)

1) The MLSI-CR11 is set for lo-true.

2) Following are jumper changes to set hi-true for Documation card readers:

DELETE :		ADD :	
J	2 - 3	J	1 - 2
K	2 - 3	K	1 - 2
K	4 - 5	K	5 - 6
L	2 - 3	L	1 - 2
L	4 - 5	L	5 - 6
M	2 - 3	M	1 - 2
M	4 - 5	M	5 - 6
		J	5 - 6

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