COMPONENTS AND SYSTEMS

FOR YOUR LSI-11

TBC Terminator/Bootstrap/Clock

User's Manual

GENERAL
ROBOTICS
CORPORATION

General Robotics Corporation

TBC USER MANUAL

740-1006-F0

Revision Table

DATE	DESCRIPTION
NOV 80	ADD DC-DC CONVERTER
SEP 81	ADDS ALL Q-BUS FINGERS
FEB 82	TERMINATE BITS 18-21
MAR 82	CORRECTIONS
OCT 82	IMPROVE DC-DC CIRCUIT
MAR 83	POWER SENSE=359MS, DROPOUT TO 1 1/2 CYCLES
OCT 83	UPDATE
AUG 84	REVISION
JAN 85	UPDATE

NOTE: Date indicates current level of manual revision.

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1. GENERAL DESCRIPTION

1.1 Introduction

The TBC (Terminator/Bootstrap/Clock) module is a dual-height, LSI-11*, QBUS* compatible module. The TBC contains most of the support functions required when integrating an LSI-11 computer system. The TBC was designed to operate in a General Robotics backplane configuration, as well as other backplanes capable of accepting LSI-11 QBUS compatible modules.

1.2 Purpose and Use

The last module in a QBUS backplane must be a terminator which provides a 220 Ohm impedance for the QBUS. The TBC provides termination for 22 address bits and various other lines as required by DEC* specifications.

The processor module requires power sequencing signals in order to initialize itself and other modules when the power is turned on. The TBC provides BPOK and BDCOK signals for proper power-up sequencing. The TBC module also has a power status LED and optional cable connections to provide remote power status indication.

Space is provided for two 8-bit EPROMS or PROMS to be used for a bootstrap. Their addressing is set to respond to 773000(8) with a window size of 256(10) words. The window size may be changed to 512,1024, or 2048 words and the address may be placed at any multiple of the window size in the I/O page by modifying a set of jumpers on the board. EPROMS of the 2704/2708/2716 family or equivalent may be used. General Robotics offers several standard EPROM sets which bootstrap multiple devices including RX02, RK05, RP02, RL02, many 8" and 5 1/4" winchester disk subsystems, SMD disk subsystems, and non-standard high density floppy disk subsystems. Custom EPROM sets are available on special request at additional charge. Options also provide for changes in the EPROM starting address and the window size in the memory map.

The TBC provides for an optional remote console panel which includes a processor RUN status indicator, RUN ENABLE/HALT switch, and options for a Line Time Clock (LTC) switch, a Bootstrap switch, and a DC power status indicator. The standard option provided by GRC includes a 15" cable assembly with a switch bracket containing the RUN ENABLE/HALT switch and an integral RUN indicator lamp. The cable has sufficient wires to allow all console options.

*TM of Digital Equipment Corporation

The TBC has a Line Time Clock (LTC) which, when activated, generates an interrupt on the BEVENT line of the CPU. The LTC is turned on by software when using RT11 V3.0 or later. Options provide for an external clock input, an external clock enable, and interrupt line (BIRQ L) rather than event line (BEVENT L) stimulation. Line time clock signals come from an external 24 VAC center-tapped transformer linked to the 50 or 60 Hertz AC power.

1.3 Description

This section contains a general description of the physical, electrical, and performance specifications of the TBC. For more detailed information, refer to sections 2, the Block Diagram in Fig. 1, and the layout diagram Fig. 3.7. .

1.3.1 Physical Description

The TBC comforms to standards for LSI-11 compatible modules, based on Digital Equipment Corporation standards for dual height modules.

The TBC is a dual height module designed to fit in a General Robotics, DEC, or any other LSI-11 QBUS compatible backplane. The module is a two layer, computer grade, printed circuit board conforming to the highest standards of quality control. The module has one 3 pin connector for receiving 24 VAC from an external source for the Line Time Clock (J1). It also has a 2x5 pin connector (J2) to provide external controls and indicators, such as a Line Time Clock, a RUN ENABLE/HALT switch, and the RUN indicator lamp. A DC Power OK LED is installed near the front edge of the module adjacent to J1 (24 VAC) and J2 (console cable).

1.3.2 Electrical Description

The TBC conforms to specifications for LSI-11 compatible modules. Connections provided to interface the module to the QBUS are LSI-11 compatible. Connections for remote console functions are provided by a 10 pin header J2. Power line signals for the power sequencing circuits and the Line Time Clock are provided through the 3 pin connector J1. See section 3 for a detailed description of the QBUS and auxiliary signals.

1.3.3 Performance

Several functions, such as power sequencing, remote switch panels, bootstrapping, and bus termination are required in most system applications. The TBC combines all these functions on a dual-wide module, freeing the system designer from additional requirements for terminator boards, controllers with built-in bootstraps, remote console modules, and other various system requirements. The TBC provides options for all of these functions, incorporating a wide range of system configurations.

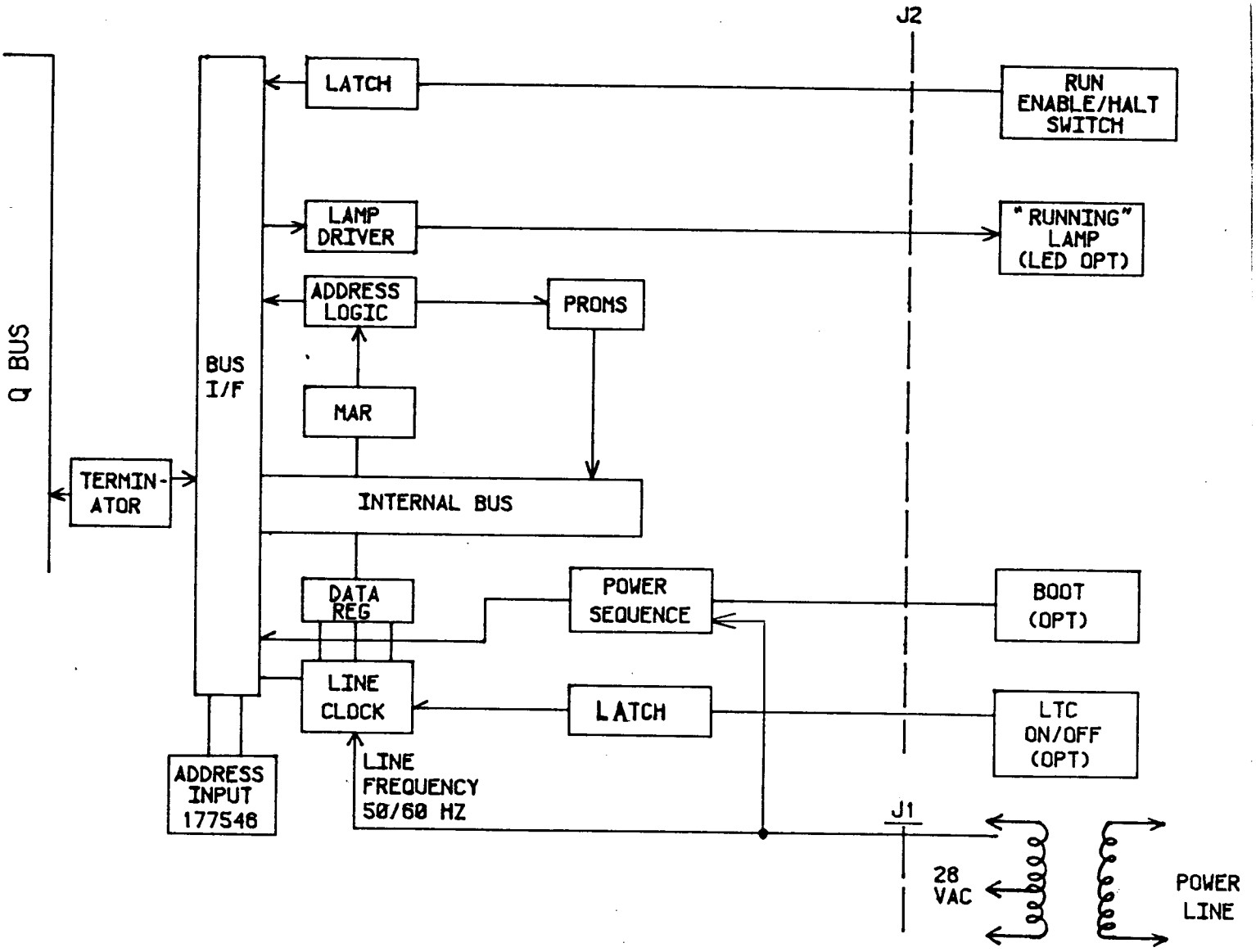


Figure 1 - Block Diagram

2. OPERATION

2.1 Introduction

This section describes the specific environmental and power requirements for the TBC module. Included are definitions of the QBUS and auxiliary signals.

2.2 Operating Requirements

2.2.1 Environmental

The following temperature and humidity specifications should be adhered to in order to ensure proper operation of the TBC module.

Storage Temperature

5 to 65 degrees C (41 to 149 degrees F)

Operating Temperature

5 to 60 degrees C (41 to 140 degrees F)

Humidity

10 to 95 % (non-condensing)

Air flow should be maintained across the module to ensure maximum temperature rise across the board of 5 degrees C (9 degrees F).

2.2.2 Power

Power required by the TBC module as measured at the backplane connection is as follows:

+5 VDC $\pm$ 5% at 1.0 Amp
+12 VDC $\pm$ 3% at 0.1 Amp

Power required by the TBC module as measured at J1 is as follows.

24 VAC-CT $\pm$ 20% at .03 Amp

2.3 Signal Definitions

Table 2.1 defines the signals between the TBC module and the QBUS. Table 2.2 defines signals on J1. Table 2.3 defines the signals on connector J2.

Table 2.1 - Signals Between TBC11 and QBUS

BUS PIN	MNEMONIC	DESCRIPTION
AA1	BIRQ5L	Not Used
AB1	BIRQ6L	Not Used
AC1	BDAL16	Not Used
AD1	BDAL17	Not Used
AF1	SSPARE2	Special Spare (SRUNL KDF11-AA LSI-11/73). This pin is tied to AH1 on 11/02 and 11/23 CPU modules. Backplane pins AF1 and AH1 must be tied together on the backplane when using a 11/73 CPU. This should be done on slot one only.
AH1	SRUNL	This signal is asserted when the processor is in a run state. It is used by the TBC to drive the run light. This pin is a special spare and is not bussed on the DEC backplanes, but is bussed on GRC's backplane. Used by LSI-11/02 and LSI-11/23. Pin AH1 tied to AF1 on these modules.
AJ1	GND	Ground - System signal ground and DC return.
AM1	GND	Ground - System signal ground and DC return.
AN1	BDMR L	Not Used
AP1	BHALT L	Processor Halt - When BHALT L is asserted, the processor responds by halting normal program execution. External interrukpts are ignored, but memory refresh interrupts (enabled if W4 on the processor module, KD11-F only, is removed) and DMA request/grant sequences are enabled. When in the halt state, the procesor executes the ODT microcode and the console device operation is invoked. --CAUTION-- The user must avoid multiple DMA data that could delay refresh transfers (burst or "hog" mode) operation. Complete refresh cycles must occur once every 1.6 ms if required.

AT1	GND	Ground - System signal ground and DC return.
BA1	BDCOK H	DC Power OK - TBC generated signal that is asserted when there is sufficient DC voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK - Asserted by the TBC when primary power is normal. When negated during processor operation, a power-fail trap sequence is initiated.
BC1	DAL18L	Not Used
BD1	DAL19L	Not Used
BE1	DAL20L	Not Used
BF1	DAL21L	Not Used
BJ1	GND	Ground - System signal ground and DC return
BK1	EXT CLK	
BM1	GND	Ground - System signal ground and DC return
BN1	BSACK L	Not Used
BP1	BIRQ7L	Not Used
BR1	BEVNT L	External Event Interrupt Request - When asserted, the processor responds (if PS Bit 7 is 0) by entering a service routine via vector address 100. A typical use of this signal is a line time clock interrupt. The 11/23 processor arbitrates as a level 6 interrupt.
BT1	GND	Ground - System signal ground and DC return
BV1	+5	+5 V Power - Normal +5 V DC system power
AA2	+5	+5 V Power - Normal +5 V DC system power
AC2	GND	Ground - System signal ground and DC return
AD2	+12	+12 V Power - +12 V DC system power
AE2	BDOUT L	Data Output - BDOUT, when asserted, implies that valid data is available on BDAL<0:15>L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.

AF2	BRPLY L	Reply - BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transactions. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted outupt data from the bus.
AH2	BDIN L	Data Input - BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and it requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew data from BRPLY L.
AJ2	BSYNC L	Synchronize - BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL<0:21>L if an 11/23 or BDAL<0:15>L if an 11/2. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte - BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
AL2	BIRQ4L	Interrupt Request - A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L. (Priority 4 with 11/23)
AM2	BIAKI L	Interrupt Acknowledge Input
AN2	BIAKO L	Interrupt Acknowledge Output If an 11/2 - This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRO L, the device will pass BIAKO L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin. If an 11/23 - In accordance with interrupt protocol, the processor asserts BIAKO L to acknowledge receipt of an interrupt. The bus transmits this to BIAKI L of the device electrically closest to the processor. This device

accepts the acknowledge under two conditions: 1) The device requested the bus by asserting BIRQXL, and 2) the device has the highest priority interrupt request on the bus at that time.

If these conditions are not met, the device asserts BIAKO L to the next device on the bus. This process continues in a daisy-chain fashion until the device with the highest interrupt priority receives the interrupt acknowledge signal.

AP2 BBS7 L — Bank 7 Select - The bus master asserts this signal to reference the I/O page (including that portion of the I/O page reserved for nonexistent memory). The address in BDAL<0:12>L when BBS7 L is asserted is the address within the I/O page.

AR2 BDMGI L

AS2 BDMGO L — DMA Grant Input and DMA Grant Output - This is the processor-generated daisy-chained signal which grants bus to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDGMO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle.

--CAUTION--

DMA device transfers must be single transfers and must not interfere with the memory refresh cycle if BREF L is used.

AT2 BINIT L — Initialize - BINIT L is asserted by the processor to initailize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).

AU2 BDAL0 L

AV2 BDAL1 L — Data/Address Lines - These two lines are part of the data/address bus over which address and data information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to, the addressed slave device or memory over the same bus lines.

BA2	+5	+5 V Power - Normal +5 V DC system power.
BC2	GND	Ground - System signal ground and DC return
BD2	+12	+12 V Power - +12 V System Power
BE2	BDAL2 L	Data/Address Lines - These 14 lines are part of the data/address bus previously described.
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

Table 2.2 - J1 Signal Definitions

Pin	Signal	Function
1	24 VAC-2	Provides one side of a center-tapped transformer signal at 24 VAC. Used for Line Time Clock and Power Sequence circuits.
2	GND	Ground point for the center tap of the 24 VAC center-tapped transformer described above.
3	24 VAC-1	Provides alternate side of the center-tapped transformer described above.
		Additional data on the use of the external cables J1 and J2 can be found in section 3.

Table 2.3 - J2 Signal Definitions

Pin	Signal	Function
1	LTC ON	When connected to ground, provides a front panel LTC enable.
2	BOOT	When momentarily tied to ground, provides resequencing of power detect circuits. The net effect is initiating a system bootstrap.
3	RUN	When connected to ground, provides front panel RUN function for a RUN ENABLE/HALT switch.
4	DC ON	Provides a 5 VDC signal indicating that the DC power supplies are on. This is the same function as the DC ON LED on the TBC module.
5	HALT	When connected to ground, provides the front panel HALT function for a RUN ENABLE/HALT switch.
6	LTC OFF	When connected to ground, provides a front panel LTC disable.
7	External LTC (Line Time Clock) input. (Logic levels)	
8	RUNNING	Run status for the front panel RUN lamp (LED optional). See NOTE 1.
9	+5 VDC	Power for front panel functions.
10	GND	Ground return for front panel cable.

NOTE 1: The TBC uses Q-bus signal SRUNL to operate this indicator. Refer to TABLE 2.1 for definition of Bus pins AH1 and AF1, which connect SRUNL to the TBC.

3. INSTALLATION AND CHECKOUT

3.1 Introduction

This section describes procedures for proper installation of the TBC in a QBUS system. The TBC contains several options available for the system designer and it is important to follow the installation procedures to custom fit the TBC to your system.

3.2 Unpacking and Visual Inspection

The TBC is shipped in a suitable container to prevent physical and electrical damage. It should be removed carefully, taking care to avoid damage to components and avoiding static electric discharge which may damage sensitive electronic devices. Check the TBC for missing or damaged components, a damaged circuit board, or signs of environmental damage. Any damage must be reported to the shipper and General Robotics Corporation immediately. Do not attempt to use a damaged module. Modules damaged by misuse or negligence are deemed to be out of warranty.

3.3 Installation

3.3.1 Console Panel and Cable

When shipped with a system, the TBC is supplied with a TBC switch cable assembly, usually as an integral part of the system chassis. This is also an option for a TBC shipped as a module. This assembly consists of a 10 conductor, 16 or 26 inch cable with a 10 pin connector on one end and a combination switch and indicator assembly on the other end. Figure 3-1 shows the diagram for the assembly.

Figure 3-1 TBC Switch and Cable Assembly

The switch is connected through the cable to P2 pins 3 and 5 which control the RUN ENABLE/HALT function. The indicator in the switch assembly is tied through the cable to P2 pins 9 (+5 VDC) and 8 (RUN) to provide the RUN indicator.

The connector end is designated P2 and is mated to J2 on the TBC module.

The TBC can operate without using the optional cable and switch assembly. In most cases, the RUN ENABLE/HALT circuit is set to the RUN state when power is applied, and if the front panel options are not desired, J2 can be left unconnected. It is advisable to purchase or fabricate a cable and switch assembly to use with J2 as it is very useful when integrating or troubleshooting a system.

--- CAUTION ---

Ensure that P2 is installed with the 'UP' label in the correct position (toward the component side of the module). Some connectors are not labelled and require matching arrows on the plug and connector. Some versions also have a keying tab, which prevents incorrect insertion. INCORRECT INSTALLATION OF THIS CABLE MAY CAUSE DAMAGE TO THE TBC MODULE.

Unused wires in the cable are unterminated at the switch end and require stripping and solder tinning if they are to be used. Sufficient cable is supplied to allow the user to install any available option. See Table 2.3.2 for optional signal names and pin assignments.

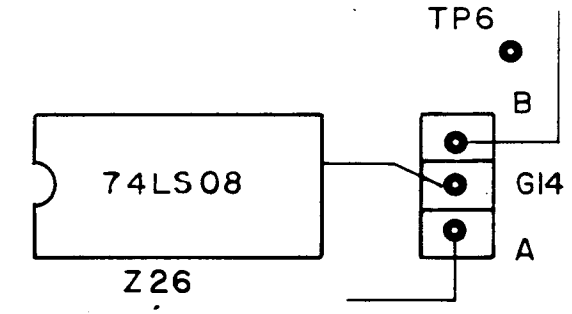
3.3.2 Console-Related Options

Some of the front panel options which are connected through J2 have additional related options on the TBC module.

3.3.2.1 Line Time Clock

If a remote Line Time Clock switch is used on the front panel, then specific jumpers are required to be installed on the TBC module.

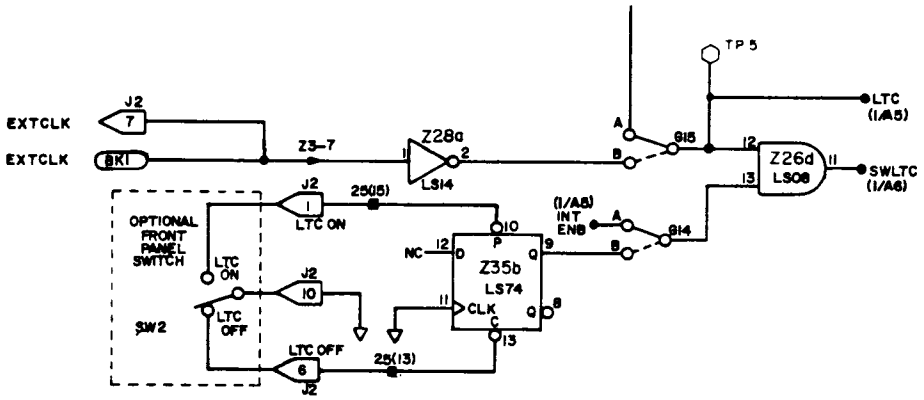
The line time clock options are factory set to allow software enabling of the LTC using the jumper from G14 to G14A. The jumper is actually a printed circuit foil between G14 and G14A on the solder side (bottom) of the TBC module. To convert to a manual (external) line time clock switch, the foil between G14 and G14A on the solder side of the module must be cut and a wire jumper installed between G14 and G14B. The holes have been placed on .1 inch centers to allow for the use of wire wrap pins and jumper plugs by the user in the event that the option is changed frequently.



ENABLE LTC OPTION

FIG. 3-2

The clock signal supplied to the module can be generated from internal or external sources. Internally, the signal comes from the circuitry which detects the AC signal from a remote 24 VAC center-tapped transformer, converts is to logic pulses in step with the power line frequency, and applies it to point G15A. The factory setting is a foil between G15 and G15A. To use the external clock, the foil between G15 and G15A is cut and a jumper wire added between G15 and G15B. The external clock can be supplied from QBUS pin BK1 or the front panel cable connector J2 pin 7.



EXTERNAL LTC OPTION

FIG. 3-3

3.3.2.2 LED and Lamp Options

Two options are available for front panel indicators. The RUN lamp is driven directly by a 75451 line driver. The circuit contains a 47 Ohm resistor for use with an LED instead of the normal incandescent lamp. The resistor (R16) has a shorting foil etched across it, which can be seen on the solder side of the module directly beneath R16. To use an LED on the front panel, cut the shorting foil. This provides current limiting for an LED indicator.

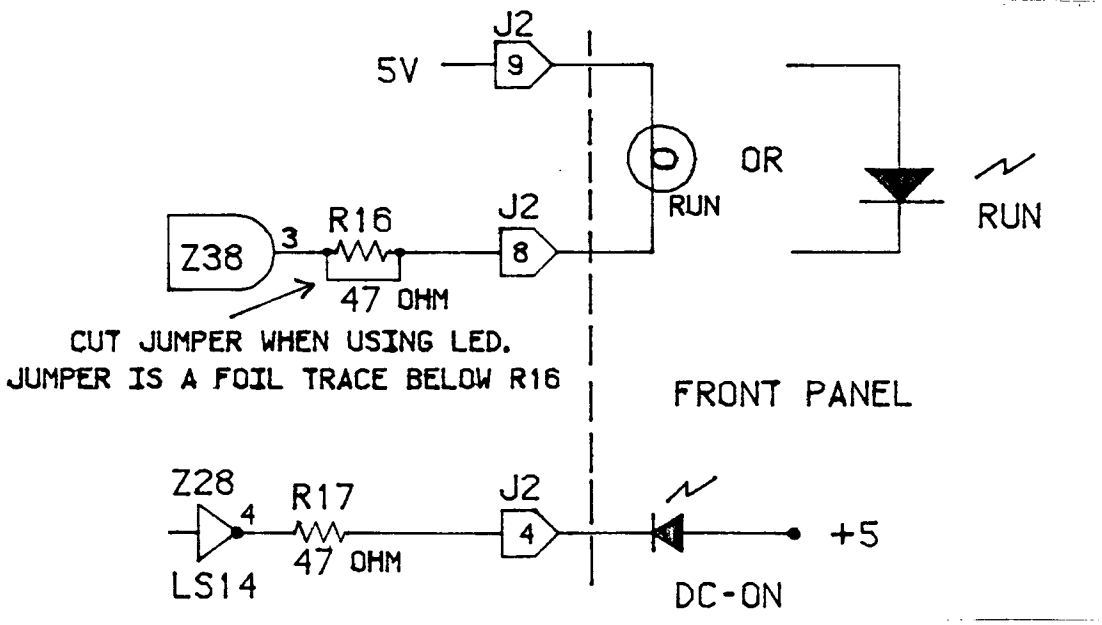


Figure 3-4 LED and Lamp Options

Note: The optional indicator for DC ON is factory set for proper operation of an LED.

Note: See section 2.3 for definition of SRUNL, which is used to operate the RUN indicator.

3.3.2.3 Boot Option

System booting can be initiated from the front panel by momentarily tying J2 pin 2 to ground. This effectively resequences the power detect circuits. The processor and other system components must be set up to Auto-Boot on power up.

3.3.3 AC Power

The Line Time Clock requires an AC signal from the power line in order to generate an interrupt on the BEVNT L line. (The clock signal may also be supplied from an external source. See paragraph 3.3.2.1)

For systems supplied by General Robotics Corporation, a small 24 VAC, center tap transformer is used to supply signals to the clock detect logic. The wires from the transformer are tied to connector J1. See Table 2.3.2

Signals from the transformer are also used to detect AC power failure, and are required to operate the TBC properly. BUS signals BDCOK and BPOK are generated on the TBC, and are used in power up sequencing. It is mandatory for proper system operation, to provide the required AC signals to J1. The user may supply his own source of AC, as long as it conforms to specifications given in Section 2.2.2. See Figure 3.5 for diagram of circuit board components. These parts may be ordered through the General Robotics Sales Office as a complete assembly.

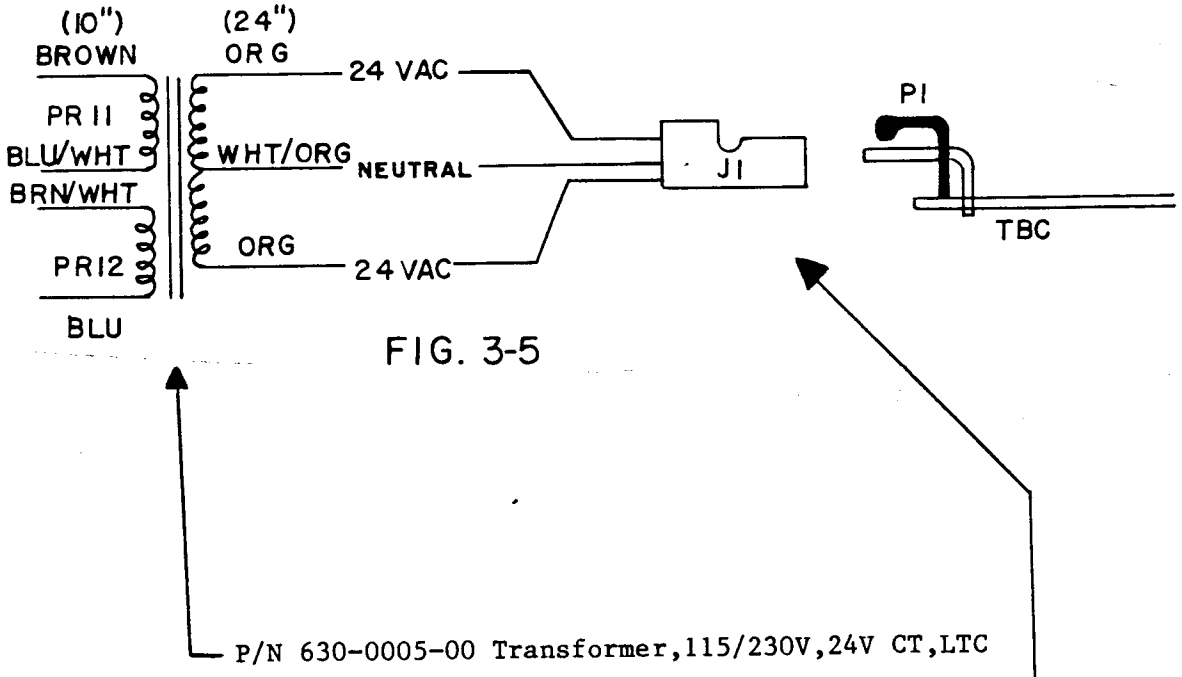
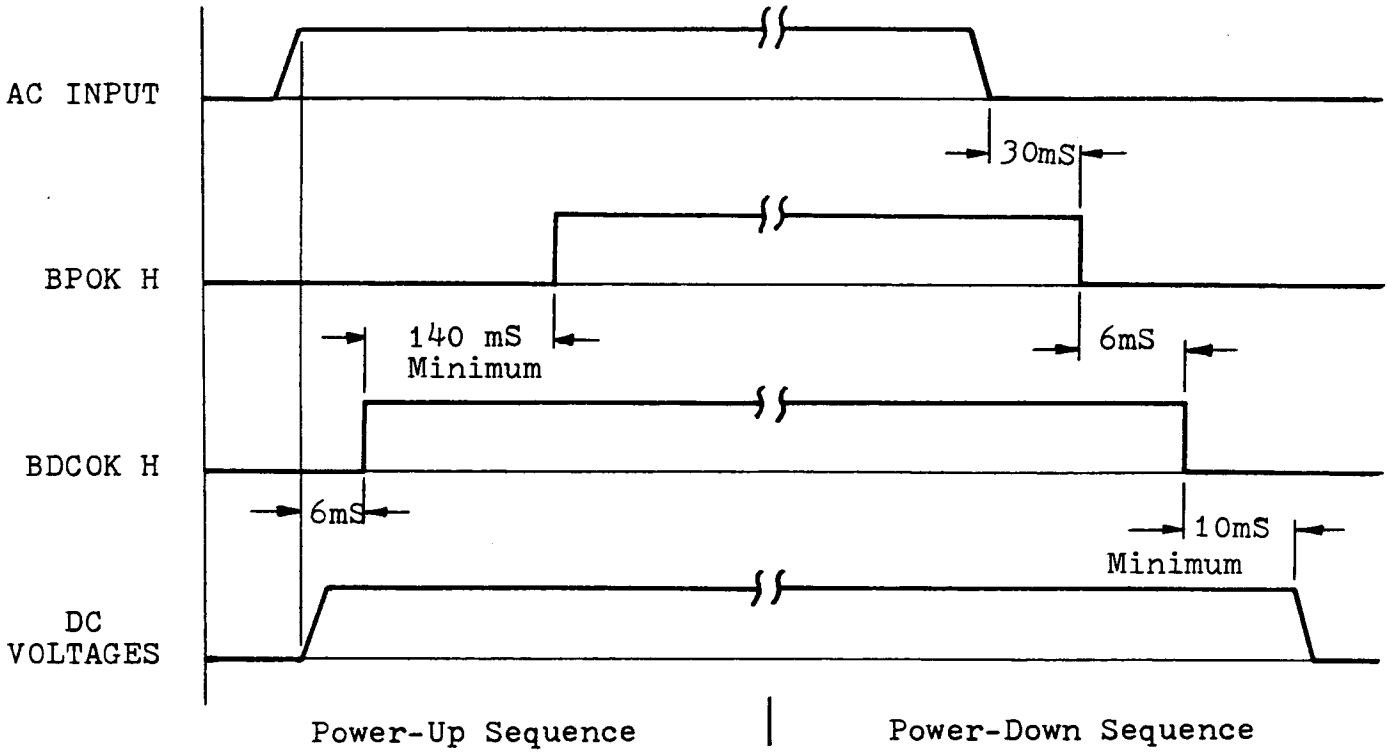


FIG. 3-5

P/N 630-0005-00 Transformer,115/230V,24V CT,LTC

P/N 676-0020-00 Connector,free hanging,3 pin,locking,male shell

P/N 682-0012-00 Connector cover,3 pin,locking



Power Signal Generation Timing
Figure 3-6

3.3.4 PROMS

Space is provided for two 8-bit EPROMS or PROMS to be used for a bootstrap. Their addressing is set to respond to 773000(8) with a window size of 256(10) words. The window size may be changed to 512, 1024, or 2048 words and the address may be placed at any multiple of the window size in the I/O page by modifying a set of jumpers on the board. EPROMS of the 2704/2708/2716 family or equivalent may be used. General Robotics offers several standard EPROM sets which bootstrap multiple devices including RX02, RK05, RP02, RL02, many 8" and 5 1/4" winchester disk subsystems, SMD disk subsystems, and non-standard high density floppy disk subsystems. Custom EPROM sets are available on special request at additional charge. Options also provide for changes in the EPROM starting address and the window size in the memory map.

To enable the bootstrap, connect the two test points at G12 and G12B with the jumper clip.

To disable the bootstrap, either:

1) Remove the jumper clip connecting G12 and G12B,

or, 2) Install the clip on only one of the test points.

See Figure 5-1 for location and identification of G12 jumper.

The following Tables provide information related to PROM options.

Table 3.1 - Power Options

Power Options	G13A	G13	G2B	G2
PROM/EPROM	TO	TO	TO	TO
Type	G13	G13B	G2	G2A
2704	IN	OUT	IN	OUT
2708	IN	OUT	IN	OUT
82S2708	OUT	OUT	OUT	OUT
2716	OUT	IN	OUT	IN *

DC = Don't Care *Normal Factory Setting

Table 3.2 - PROM Starting Address

PROM Starting Address	G6B TO G6	G6 TO G6A	G1A TO G1	G1 TO G1B	G8A TO G8	G8 TO G8B	G7B TO G7	G7 TO G7A	NOTES
00XXXX	OUT	IN	OUT	IN	OUT	IN	OUT	IN	
01XXXX	OUT	IN	OUT	IN	OUT	IN	IN	OUT	1,2
02XXXX	OUT	IN	OUT	IN	IN	OUT	OUT	IN	2
03XXXX	OUT	IN	OUT	IN	IN	OUT	IN	OUT	1,2
04XXXX	OUT	IN	IN	OUT	OUT	IN	OUT	IN	
05XXXX	OUT	IN	IN	OUT	OUT	IN	IN	OUT	1,2
06XXXX	OUT	IN	IN	OUT	IN	OUT	OUT	IN	2
07XXXX	OUT	IN	IN	OUT	IN	OUT	IN	OUT	1,2
10XXXX	IN	OUT	OUT	IN	OUT	IN	OUT	IN	1,2
11XXXX	IN	OUT	OUT	IN	OUT	IN	IN	OUT	1,2
12XXXX	IN	OUT	OUT	IN	IN	OUT	OUT	IN	2
13XXXX	IN	OUT	OUT	IN	IN	OUT	IN	OUT	1,2
14XXXX	IN	OUT	IN	OUT	OUT	IN	OUT	IN	
15XXXX	IN	OUT	IN	OUT	OUT	IN	IN	OUT	1,2
16XXXX	IN	OUT	IN	OUT	IN	OUT	OUT	IN	2
17XXXX	IN	OUT	IN	OUT	IN	OUT	IN	OUT	1,2 *

XXXX = SEE TABLE 3.3. *Normal Factory Setting

IMPORTANT NOTE: Starting with the Rev. C TBC, BBS7 enters into the equation for the starting address, which limits the PROM/EPROM starting address to the I/O page (760000 to 777777). If addressing in the range 000000 to 177777 is required, cut run to Z20 pin 5 and connect pin 5 to pin 8, and use above Table.

NOTES:

1. Starting address not available for 2708, 2716, etc. with window size of 1024. See Table 3.2. (Both G7 links out.)

2. Starting address not available for 2716, etc with window size of 2048. See Table 3.2. (All G7 & G8 links out).

Table 3.3 - PROM Window Size

PROM Window Size	G4A TO G4	G4 TO G4B	G9B TO G9	G9 TO G9A	G9C TO G9C	G9C TO G10	G10 TO G10B	G10 TO G10A	G11B TO G11
256	IN	OUT	OUT	IN	OUT	OUT	IN	OUT	OUT
512	OUT	IN	OUT	IN	OUT	OUT	IN	OUT	IN
1024	OUT	IN	IN	OUT	OUT	IN	OUT	OUT	IN
2048	OUT	IN	IN	OUT	IN	OUT	OUT	IN	IN

PROM Window Size (CONT)	G11 TO G11A	G5B TO G5	G5 TO G5A	G3A TO G3	G3 TO G3B	Used
256	IN	IN	OUT	IN	OUT	BOOT
512	OUT	OUT	IN	OUT	IN	2704
1024	OUT	OUT	IN	IN	OUT	2708
2048	OUT	OUT	IN	IN	OUT	2716

BOOT = Normal Factory Setting

Table 3.4 - PROM Address Range

PROM Address Range	G12A TO G12	G12B TO G12	G12 TO G12C	G12 TO G12D	When Used	
XX1000--XX1776	IN	OUT	OUT	OUT	--	
XX3000--XX3776	OUT	IN	OUT	OUT	BOOT	*
XX5000--XX5776	OUT	OUT	IN	OUT	--	
XX7000--XX7776	OUT	OUT	OUT	IN	--	
XX0000--XX1776	IN	OUT	OUT	OUT	2704	
XX2000--XX3776	OUT	IN	OUT	OUT	2704	
XX4000--XX5776	OUT	OUT	IN	OUT	2704	
XX6000--XX7776	OUT	OUT	OUT	IN	2704	
X00000--X03776	IN	OUT	OUT	OUT	2708	
X04000--X07776	OUT	IN	OUT	OUT	2708	
X10000--X13776	OUT	OUT	IN	OUT	2708	
X14000--X17776	OUT	OUT	OUT	IN	2708	
X00000--X07776	IN	OUT	OUT	OUT	2716	
X10000--X17776	OUT	IN	OUT	OUT	2716	
X20000--X27776	OUT	OUT	IN	OUT	2716	
X30000--X37776	OUT	OUT	OUT	IN	2716	

*Normal Factory Setting

3.3.5 Software Registers

The line time clock, when activated, generates an interrupt on the BEVNT L line, synchronized to the AC line frequency provided by the 24VAC transformer input. The clock is automatically turned on by software during the bootstrap in Version 3 (and later) of the RT-11 operating system. Options available are external clock input, external clock enable, and interrupt line (BIRQ L) rather than event line (BEVNT L) stimulation.

Since RT-11 V02 does not turn on the clock, this may be done by (1) Booting the system, (2) Halting the system, (3) Accessing location 777546, (4) Inserting the value 100 into it, and (5) Typing P to continue. Note that any time a "G" from ODT or a bus reset instruction is executed, the clock will stop and must be manually restarted.

The LTC control register is at octal address 777546 with contents as shown below:

LTCCSR: 777546

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MON	IE	S	0	0	0	0	0

BITS DESCRIPTION

15-8 Zero - Not Used.

7 MON - Monitor is set when a line time clock (LTC) pulse has occurred (every 16.67 ms for 60 hz and 20 ms for 50 hz). Reset by writing a "0" into Bit 7 or by BINIT L. Read only.

6 IE - Interrupt Enable, when set, enables interrupts from LTC. Interrupt is generated on either the BEVNT L line or the BIRO L line, depending on the state of Bit 5. Reset by writing a "0" into Bit 6 or by BINIT L. Read/Write.

5 S - Select, when set along with Bit 6 and an LTC interrupt occurs, activates the BIRQ L line. A vector of 100(8) is generated when the processor responds. When reset, under the same conditions as above, the BEVNT L line is activated. Reset by writing a "0" into Bit 5 or by BINIT L. Read/write.

4-0 Zero - Not used.

The first indication that the Line Time Clock is properly working is when correct AC and DC power is applied to the TBC module. The DC ON indicator(LED) should light. The circuits which generate the power sequence signals utilize some of the same circuits for the Line Time Clock.

After booting the system, the Line Time Clock can be tested by using the RT-11 Monitor command for displaying time. The command under RT-11 Version 3 (or later) is: .TIME (Carriage Return)

The response for time is: 00:00:00
The format for time is: HH:MM:SS

3.3.6 Backplane Position

Boards should be placed in the backplane in such a manner that backplane continuity is preserved. This requires that the slots be filled in order starting from the upper left and proceeding downward in a zig-zag pattern

with the TBC as the last board. It is allowable to place the TBC at the very end of the BUS, or at the bottom of the card cage, with open slots in the backplane. This makes it more convenient to connect and route cables to the TBC.

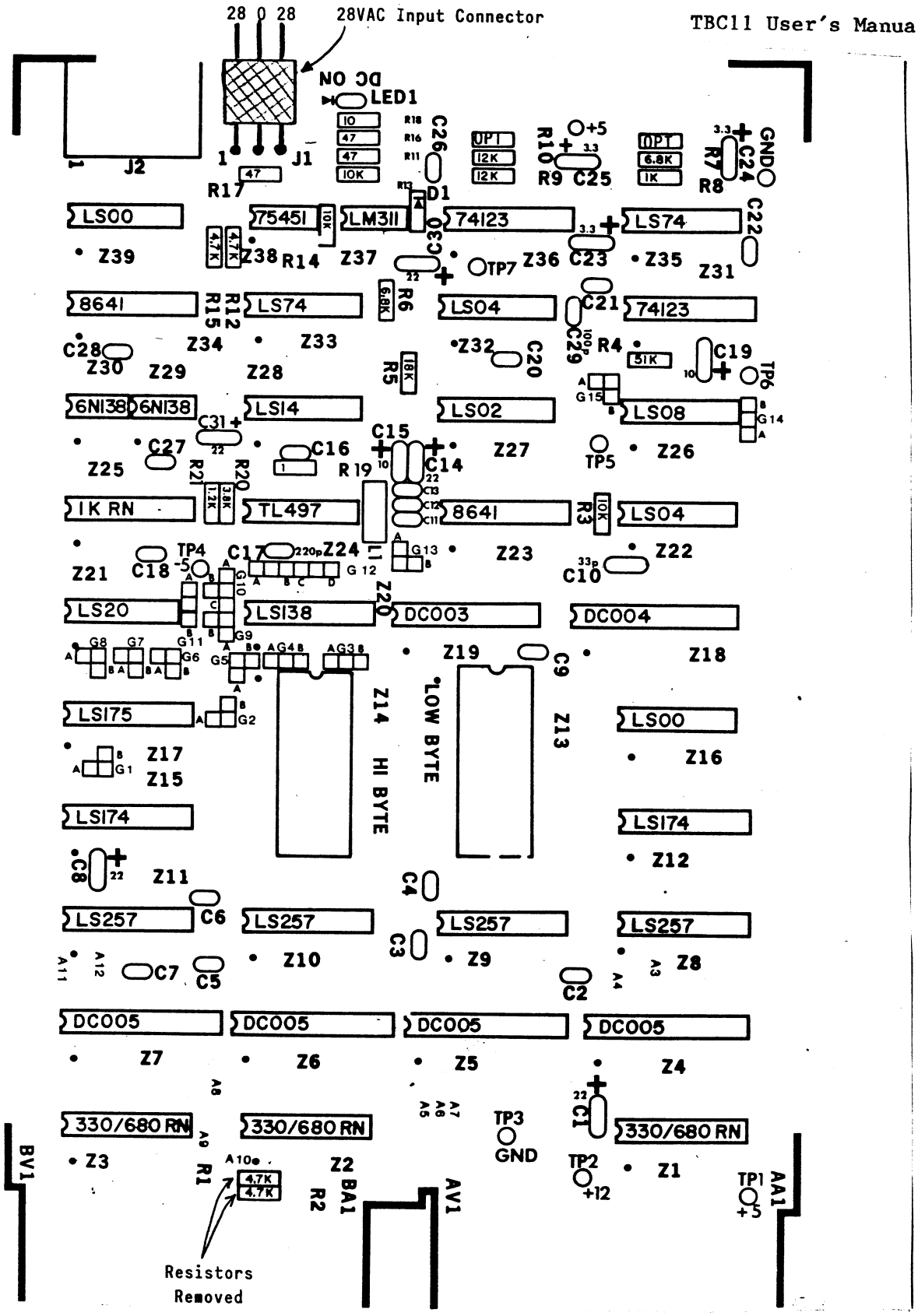


Figure 5-1 Circuit Board Layout